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Severity:
Recommended

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Increasing GR8BUS and slot-bus circuit load capacity

Background: in the default configuration the GR8BUS's address and data lines are pulled up through resistor packs of 22kOhm value located on the CPU board. They ensure that when bus signal level is high, the CPU and other devices reliably read logical 1, and when bus signal is tri-stated, there is no undefined electrical level which may cause self-oscillation causing problems at the tri-state time or after appearance of valid signal on the bus. The same mechanism is implemented in the external slot-bus, with pull-up resistor packs located on the slot board.

The issue: as you add more devices to the GR8BUS, more current is sunk off the bus lines, making it more difficult to keep a valid logical 1 level (see TTL family and CPU product specification). When bus load increases, signals' positive edges slope due to inability of 22kOhm resistor packs to provide current for quick pull-up. The problem shows up by the CPU reading wrong data from data bus, and a device attached to the GR8BUS malfunctions. In case of slot board, length of the cable between main board and slot board has an impact on the quality of the signal at the slot board's side – as long cables are prone to electrical signal reflection back to the signal's originator, and may cause unintended voltrop (voltage drop) of the signals causing issues to the signal logical level interpretation by the receiving device.

Solution: replacing CPU board's RN1, RN2 and RN4 22kOhm resistor packs with resistor packs of 10kOhm value solves the issue. Increased bus current is now able to provide the necessary positive edge rise timing, as well as logical 1 level with increased number of devices attached to the GR8BUS. For the slot board, we advise to replace 10KOhm resistor packs with 4.7KOhm resistor packs. They will provide better characteristics in terminating the bus, as well as more stable logical 1 level for longer cables. [You can reuse 10KOhm resistor packs intended for slot board in the CPU board assembly.]

Proof: this issue was identified during troubleshooting of the Nowind interface on the GR8BIT system at 3.580MHz CPU clock speed, connected to the GR8BUS converter (interface) board, and to the slot board. Extensive tests with specially designed diagnostic tools confirmed the successful issue resolution. The issue was not identified on the stage of design because devices used for testing of the design were either not consuming much current from the involved signal lines (e.g. ROM cartridge devices), or were having built-in pull-up resistors (e.g. FD-051 floppy disk controller). Please also refer to KB0002 for similar advisory on the GR8BUS converter board.

Further information:

- Wikipedia (2012) *Three-state logic*, available online at http://en.wikipedia.org/wiki/Three-state_logic (accessed on Feb 24, 2012)
- Wikipedia (2012) Transistor–transistor logic, available online at http://en.wikipedia.org/wiki/Transistor%E2%80%93transistor_logic (accessed on Feb 24, 2012)
- Zilog (2002) *Z8400/Z84C00 Z80 CPU Product Specification*, available online at http://www.zilog.com/docs/z80/ps0178.pdf (accessed on Feb 24, 2012)

KB article release notes: KB0001 was initially released on February 24, 2012, covering GR8BUS matters only. It was re-released on July 18, 2012 to cover slot board matters. Changes (additions) to the re-released version are highlighted in gray.